

GeForce6100PM-M2

REV: 2.0 (Support AM2+)

PCB:15-V09-011010

BOM:89-206-V09210

MCP61S Real S3

Components :693PCS

Add R26.R28.R29.R30

Del R48

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	Signature	Date
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Designer	Eli	07/11/2007
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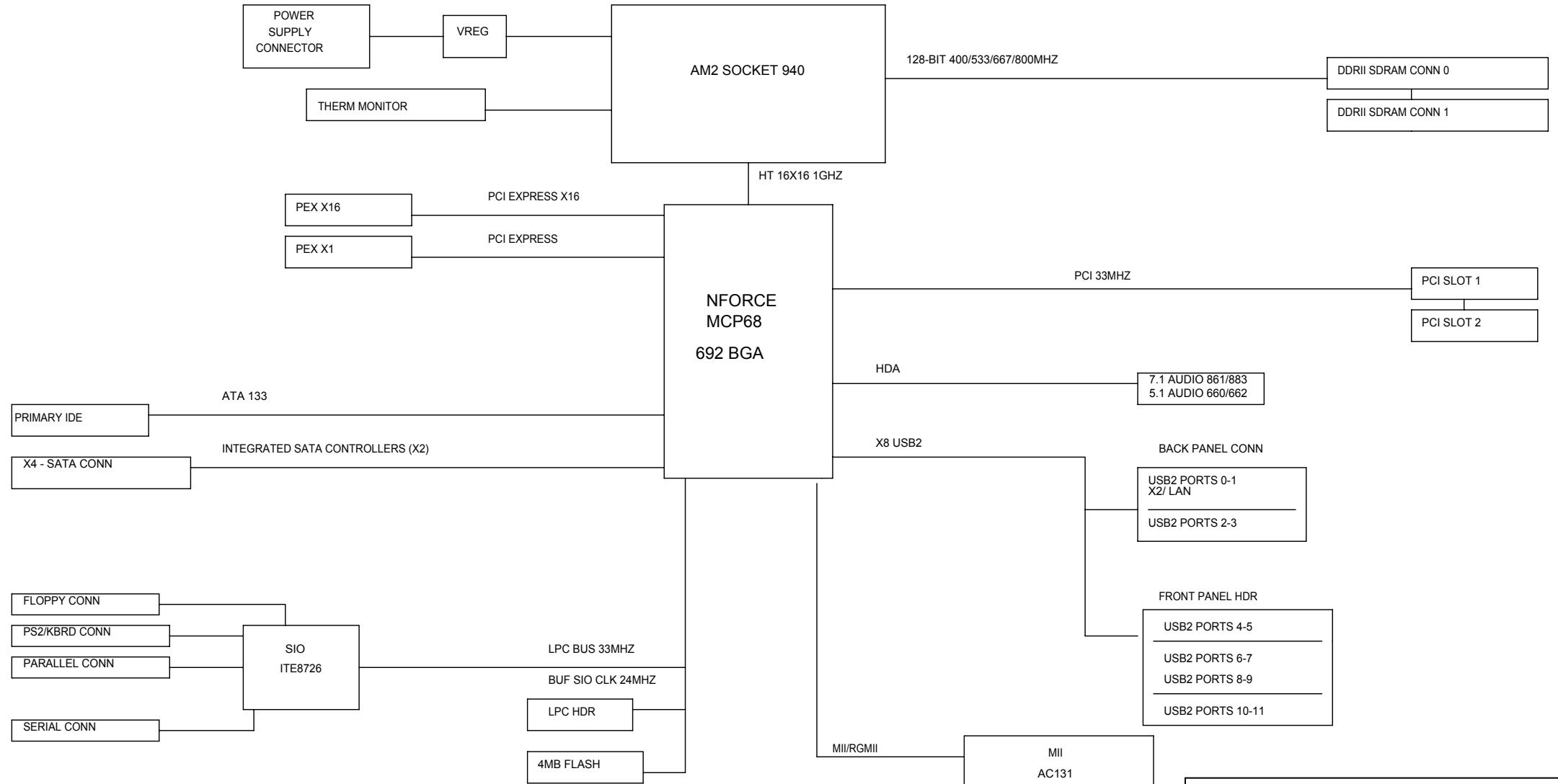
Layout	Susan/ Angela	05/29/2007
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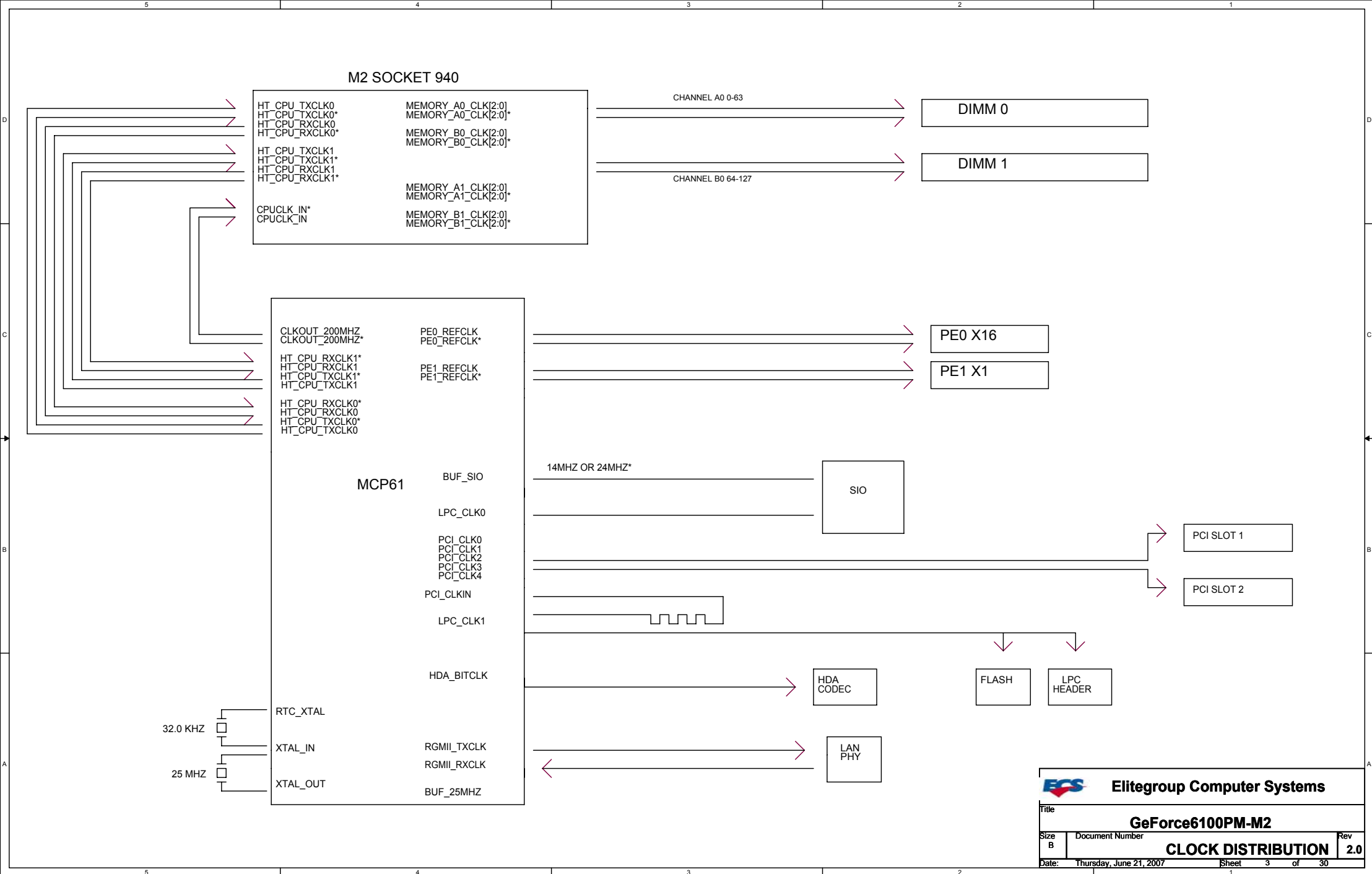
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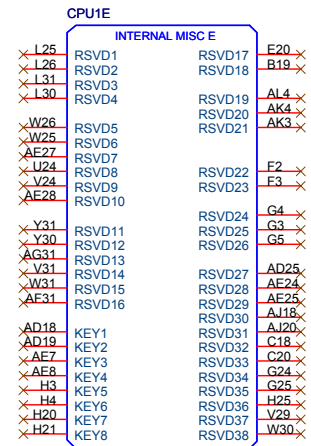
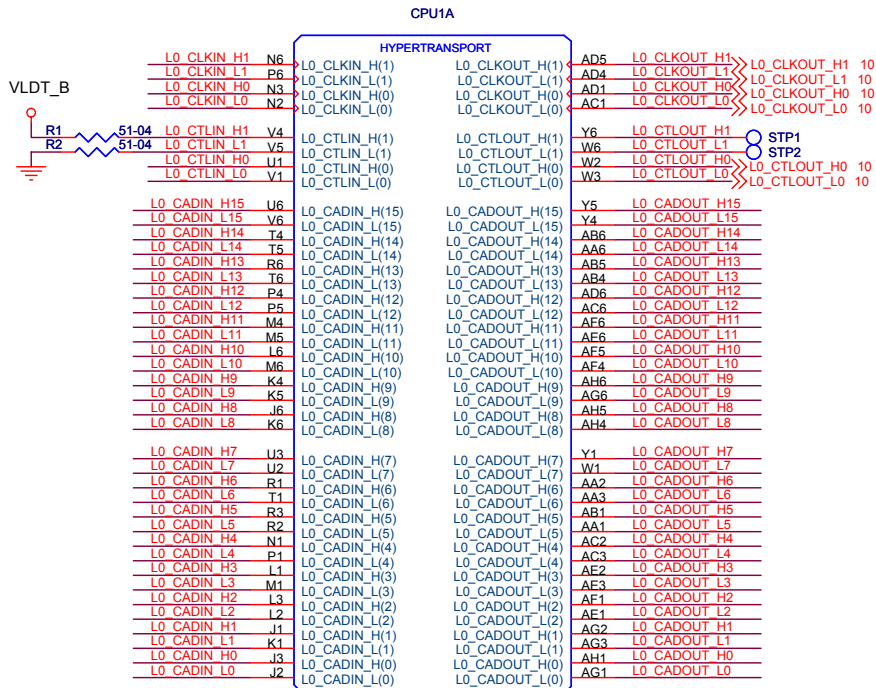
 Elitegroup Computer Systems		
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BLOCK DIAGRAM



 Elitegroup Computer Systems			
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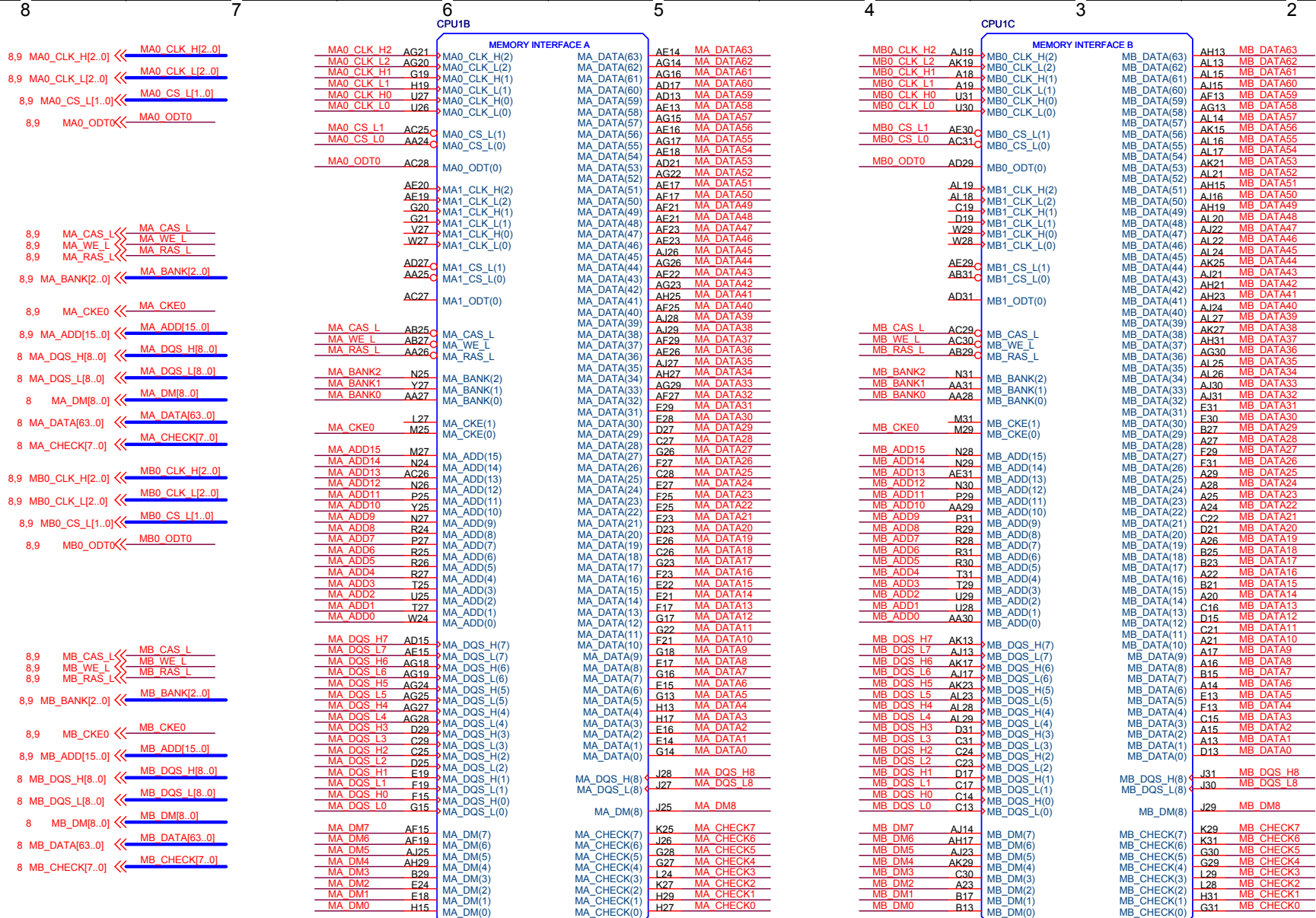




ZIF-940PS-TYC



<OrgAddr1> Elitegroup Computer Systems			
Title GeForce6100PM-M2			
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CPU M2-1 HyperTransport.0			
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ZIF-940PS-TYC

ZIF-940PS-TYC

GeForce6100PM-M2

CPU M2-2 DDR2

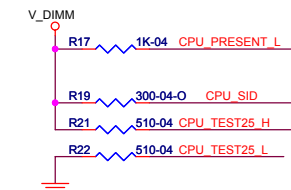
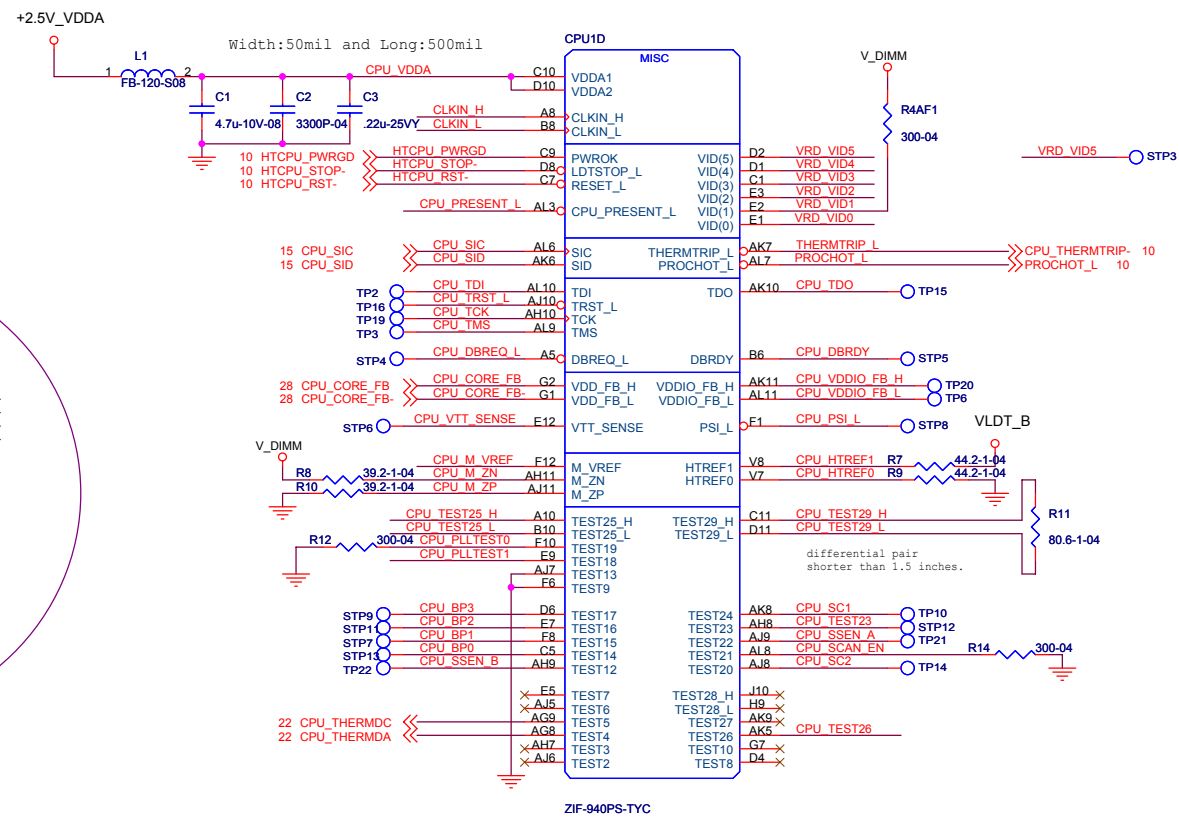
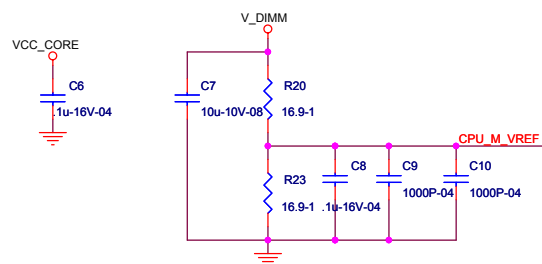
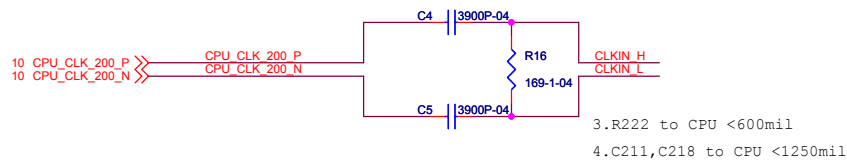
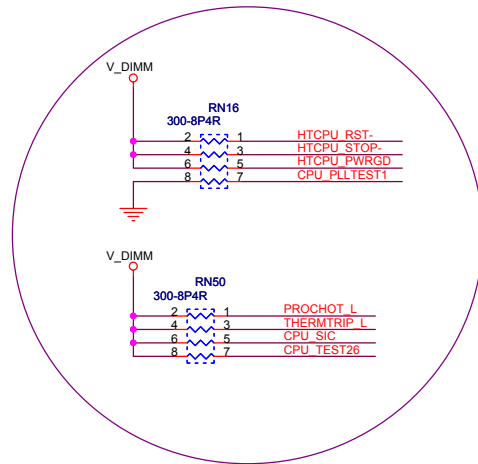
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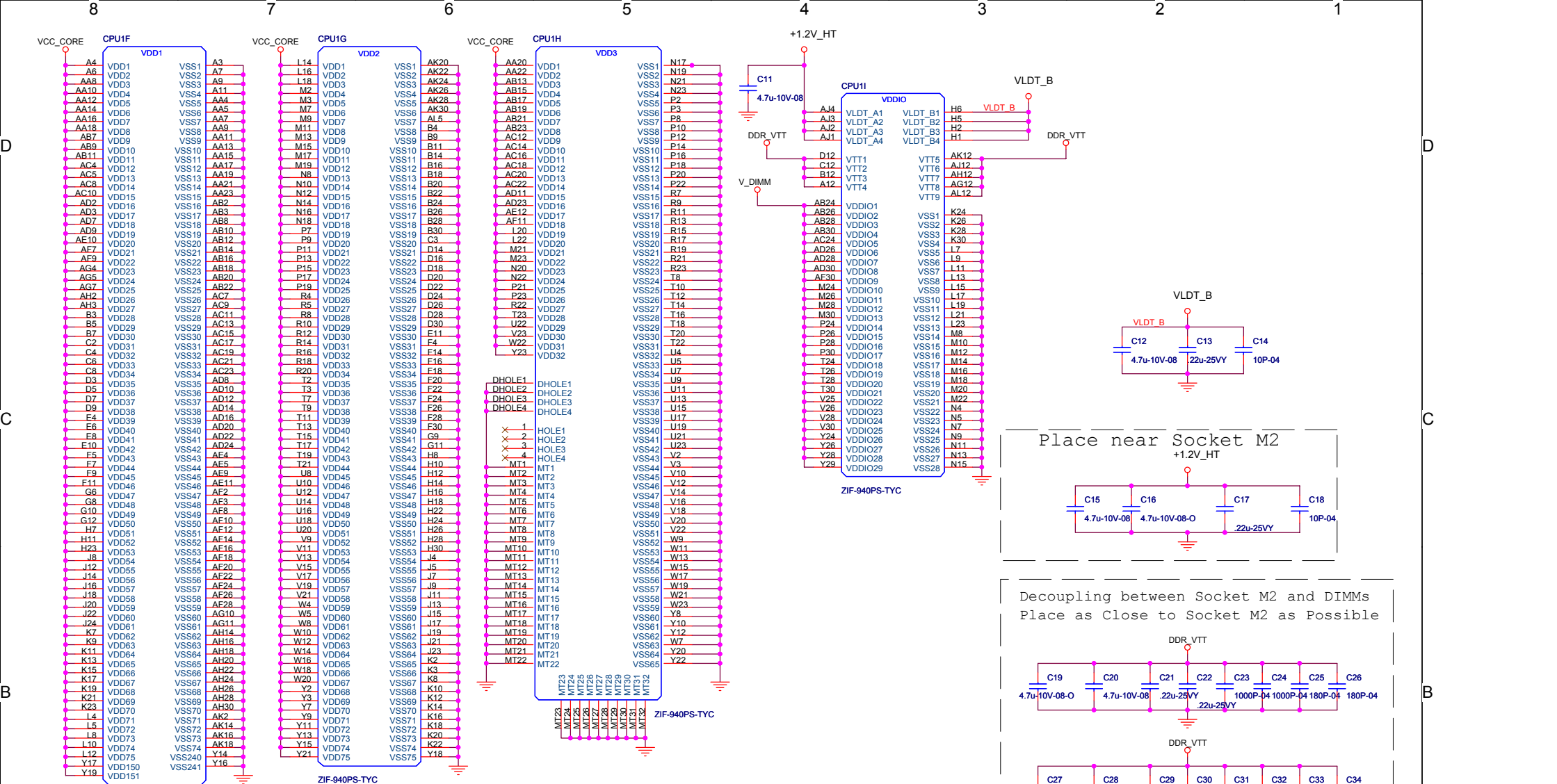
Rev 2.0

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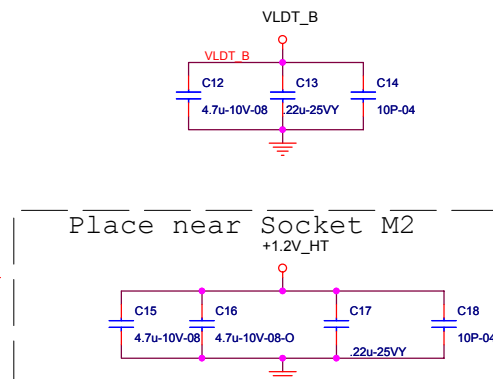
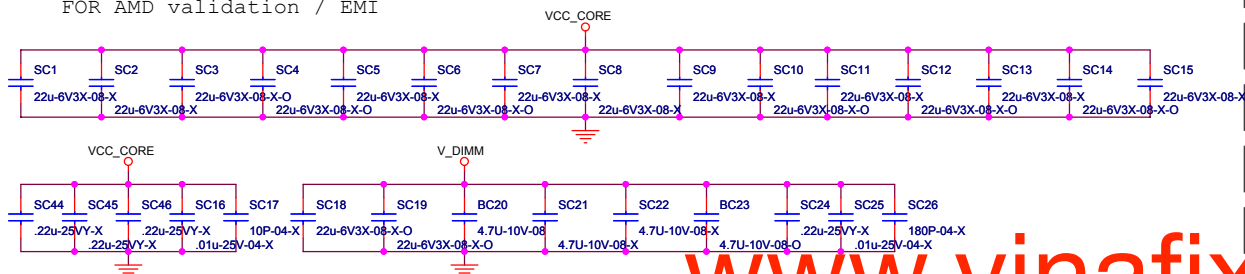
The diagram shows a circuit for generating a 2.5V voltage source. It features an operational amplifier (U2A, GS358SFS) configured as a voltage follower. The non-inverting input (+) is connected to a voltage divider consisting of a 10k resistor (R3) and a 100k resistor (R4) connected to VREF25. The inverting input (-) is connected to the output of the op-amp. The output of the op-amp (pin 1) is connected to the gate of a MOSFET (Q1, 2N7002-S). The MOSFET's source is connected to ground, and its drain is connected to the +2.5V_VDDA supply. The MOSFET is also connected to a 100nF capacitor (EC1) to ground. The +2.5V_VDDA supply is labeled with a current of 105mA.



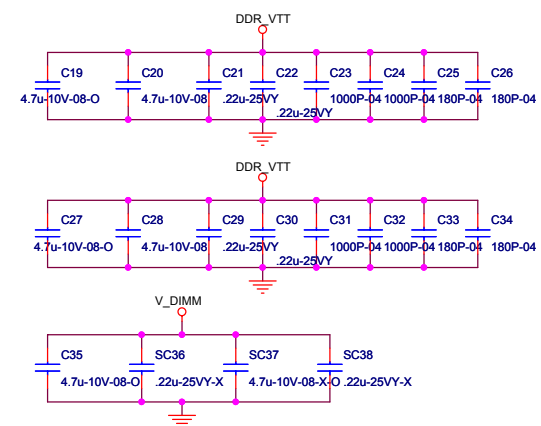


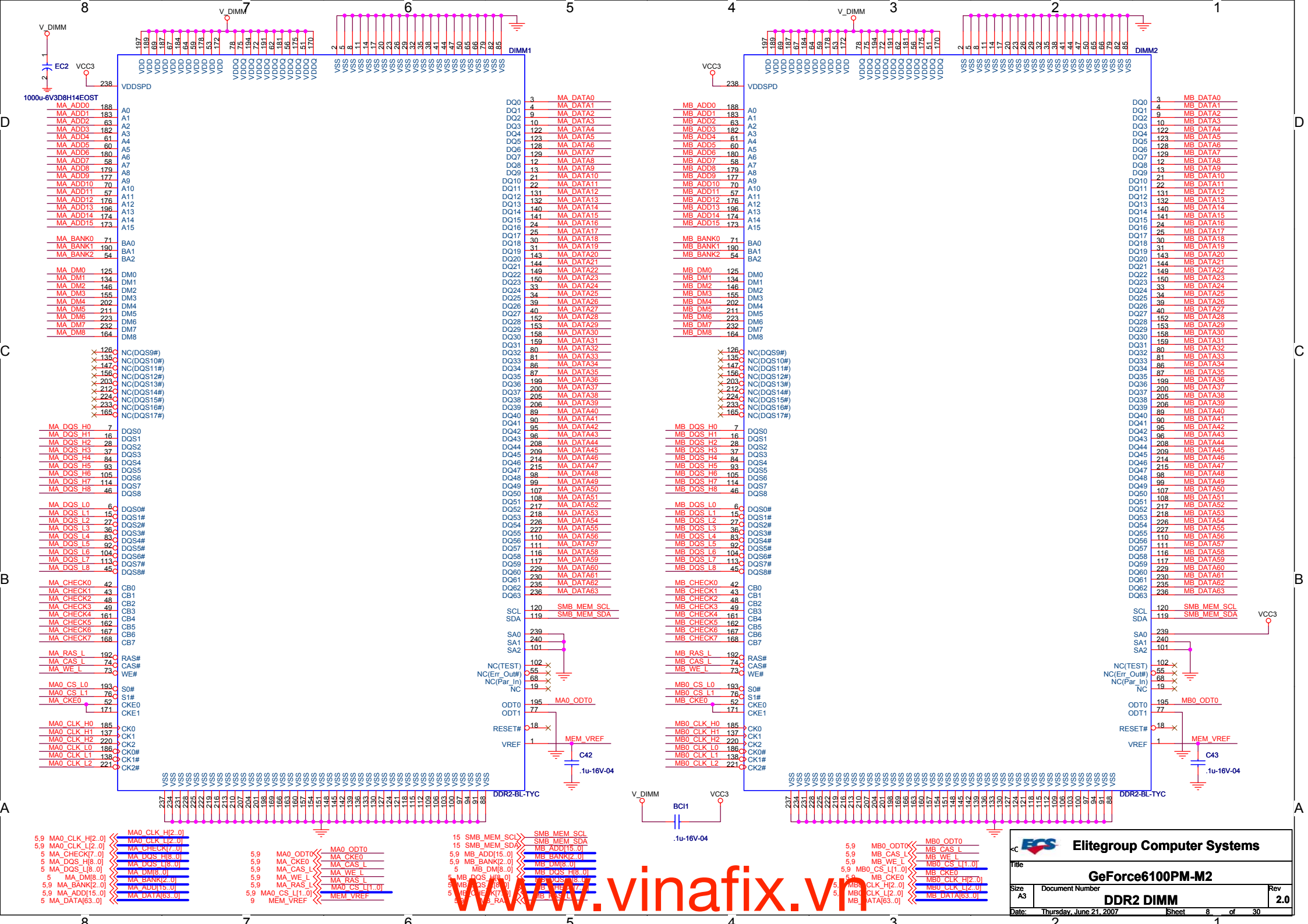
Place Decoupling Capacitors on Bottom Side underneath Socket M2

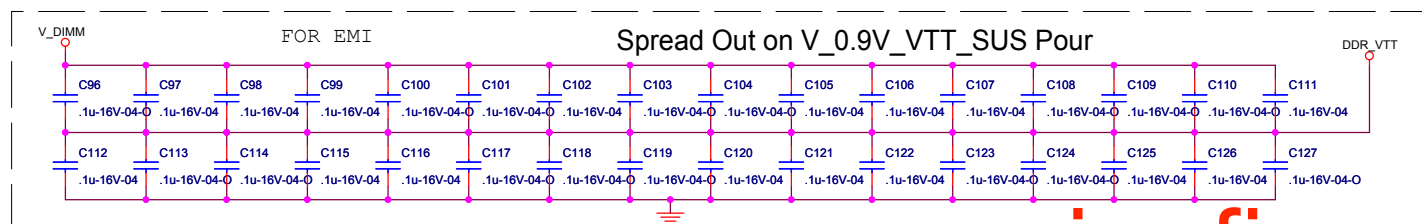
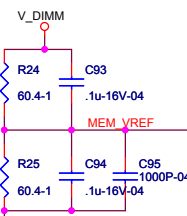
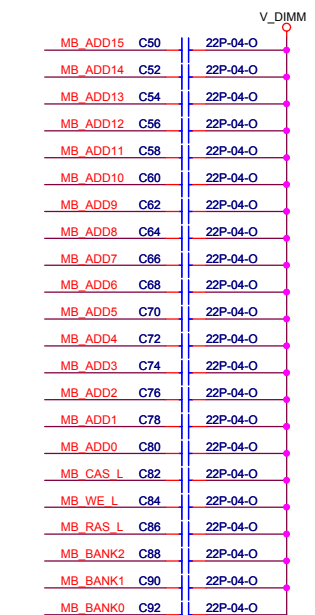
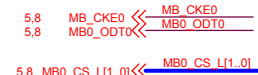
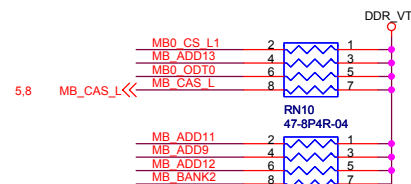
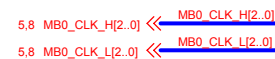
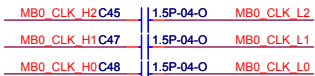
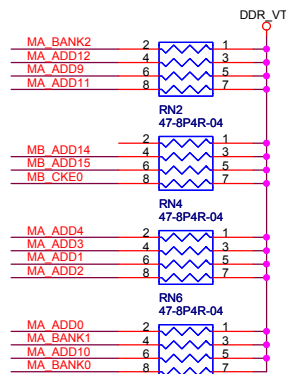
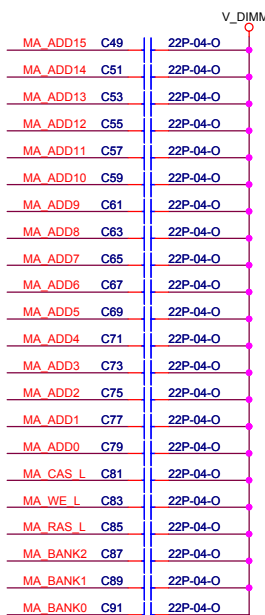
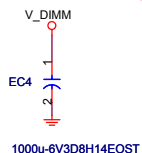
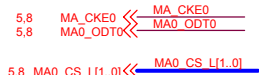
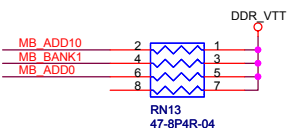
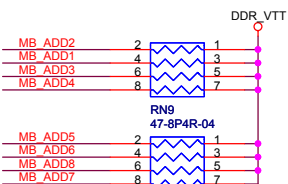
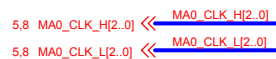
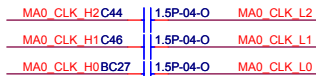
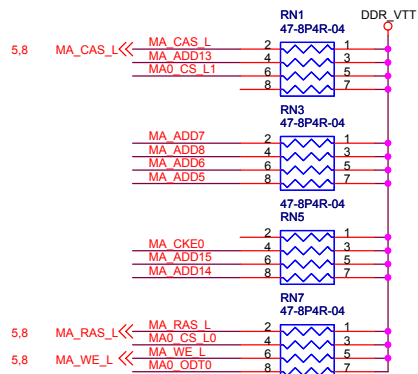
FOR AMD validation / EMI



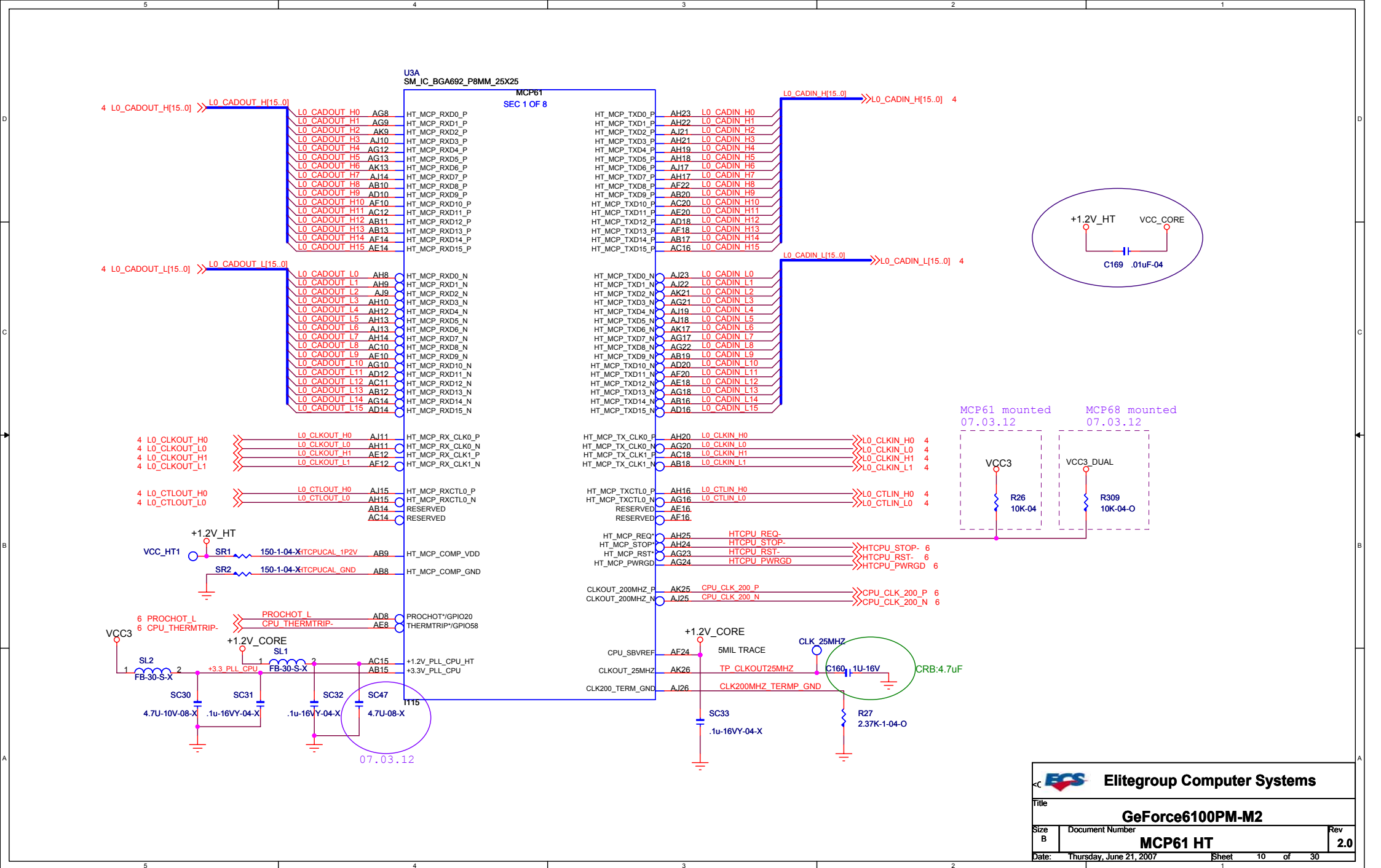
Decoupling between Socket M2 and DIMMs
Place as Close to Socket M2 as Possible

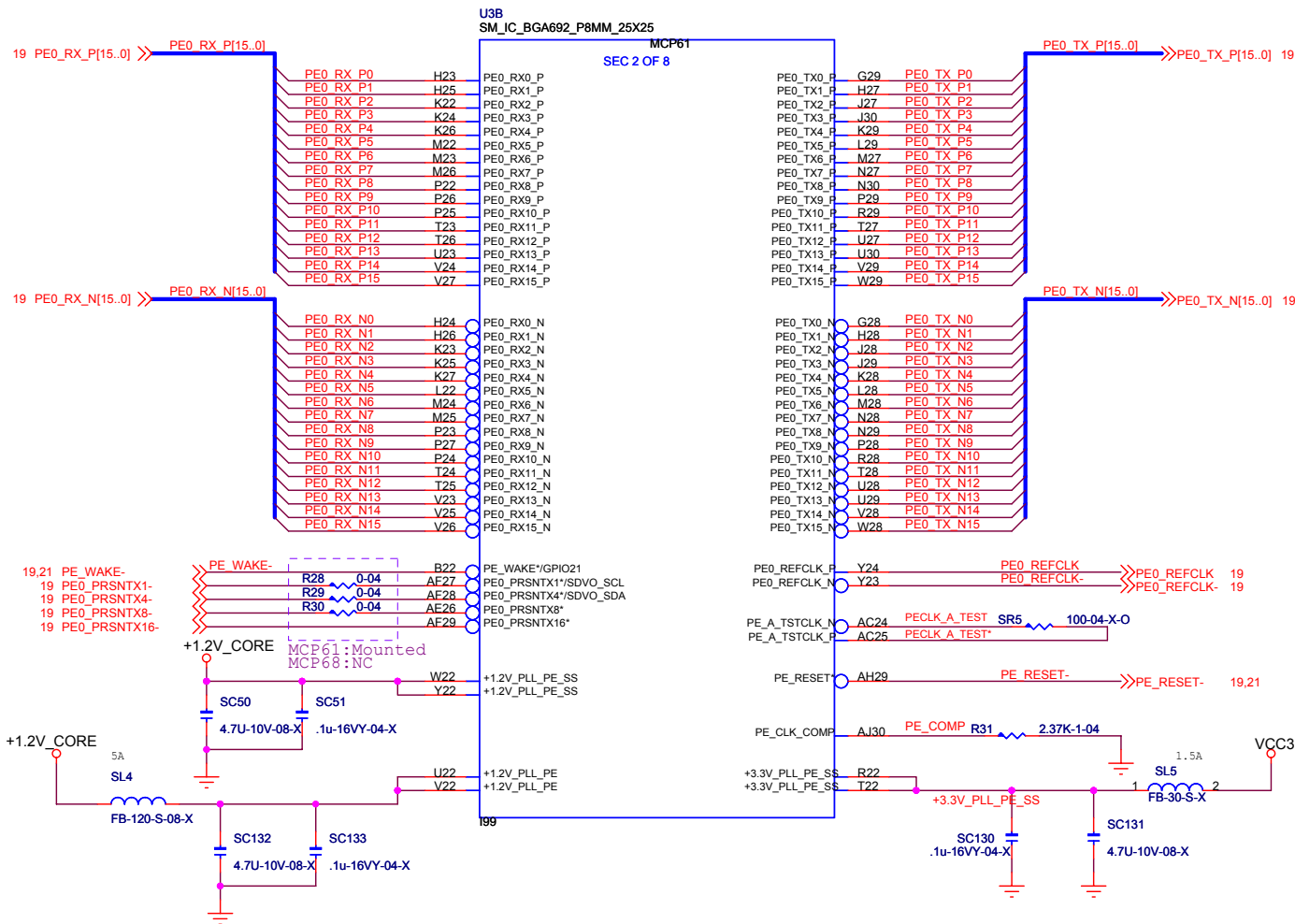






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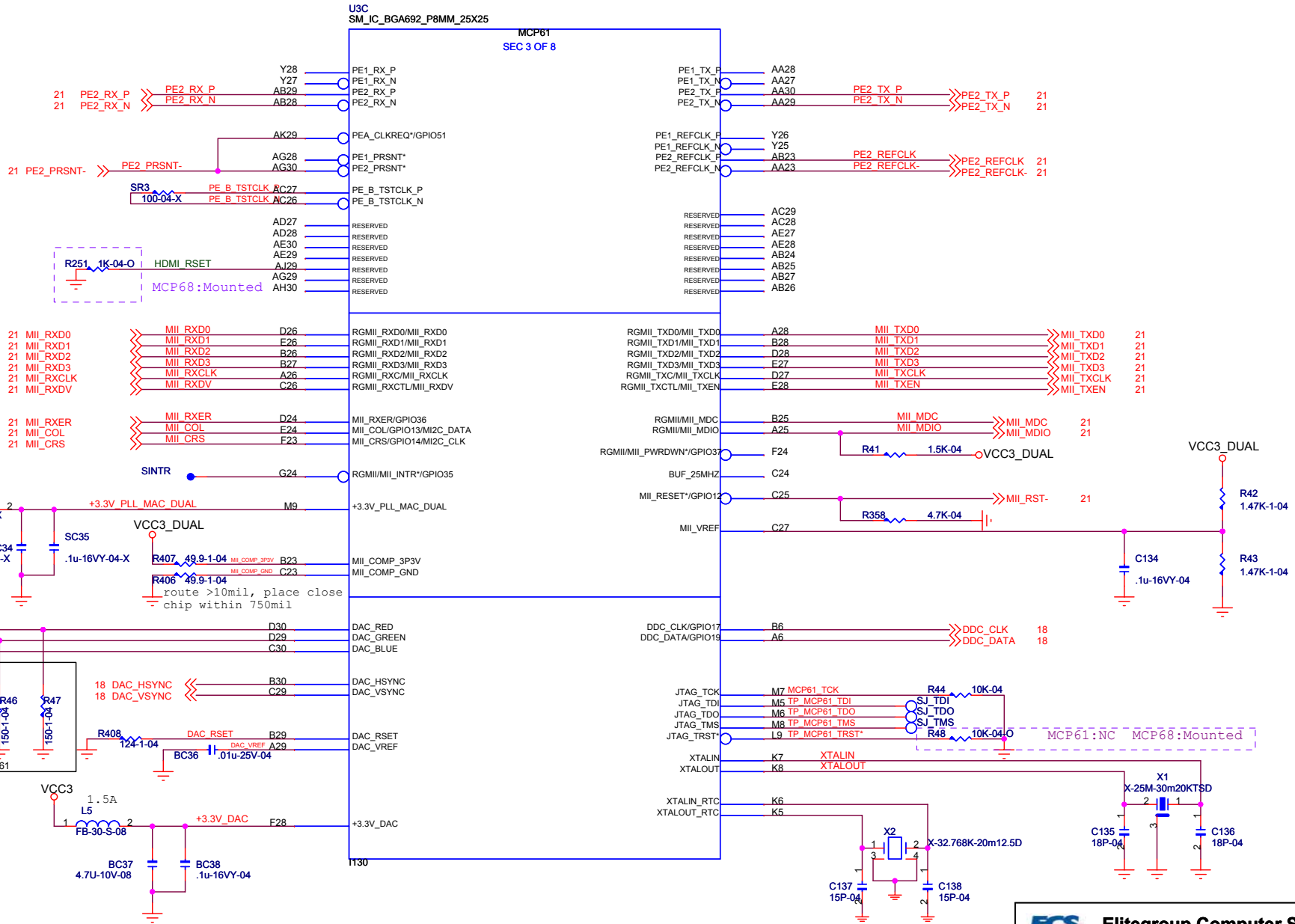
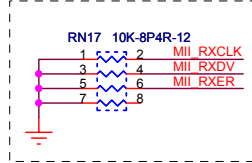




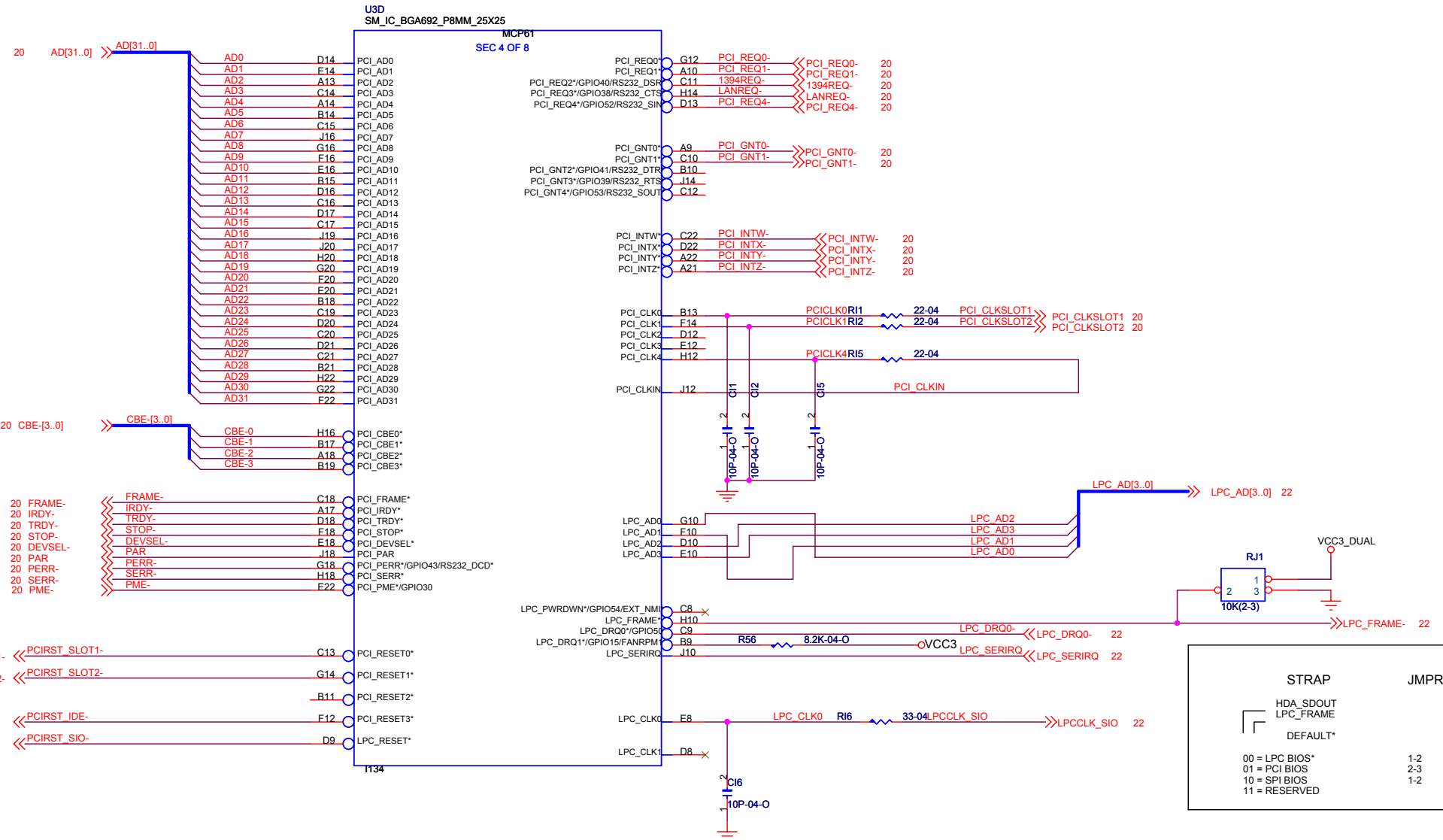
MCP61 Pin Define	MCP68 Pin Define
PRSNXTX1 (AF27)	+3.3V_HDMI_PLL_HVDD
PRSNXTX4 (AF28)	HDCP_ROM_SCLK
PRSNXTX8 (AE26)	+3.3V_HDMI
GND (AF30)	HDCP_ROM_SDATA

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	MCP61 PCI-E X16	2.0	
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For enhance AC131 Driving

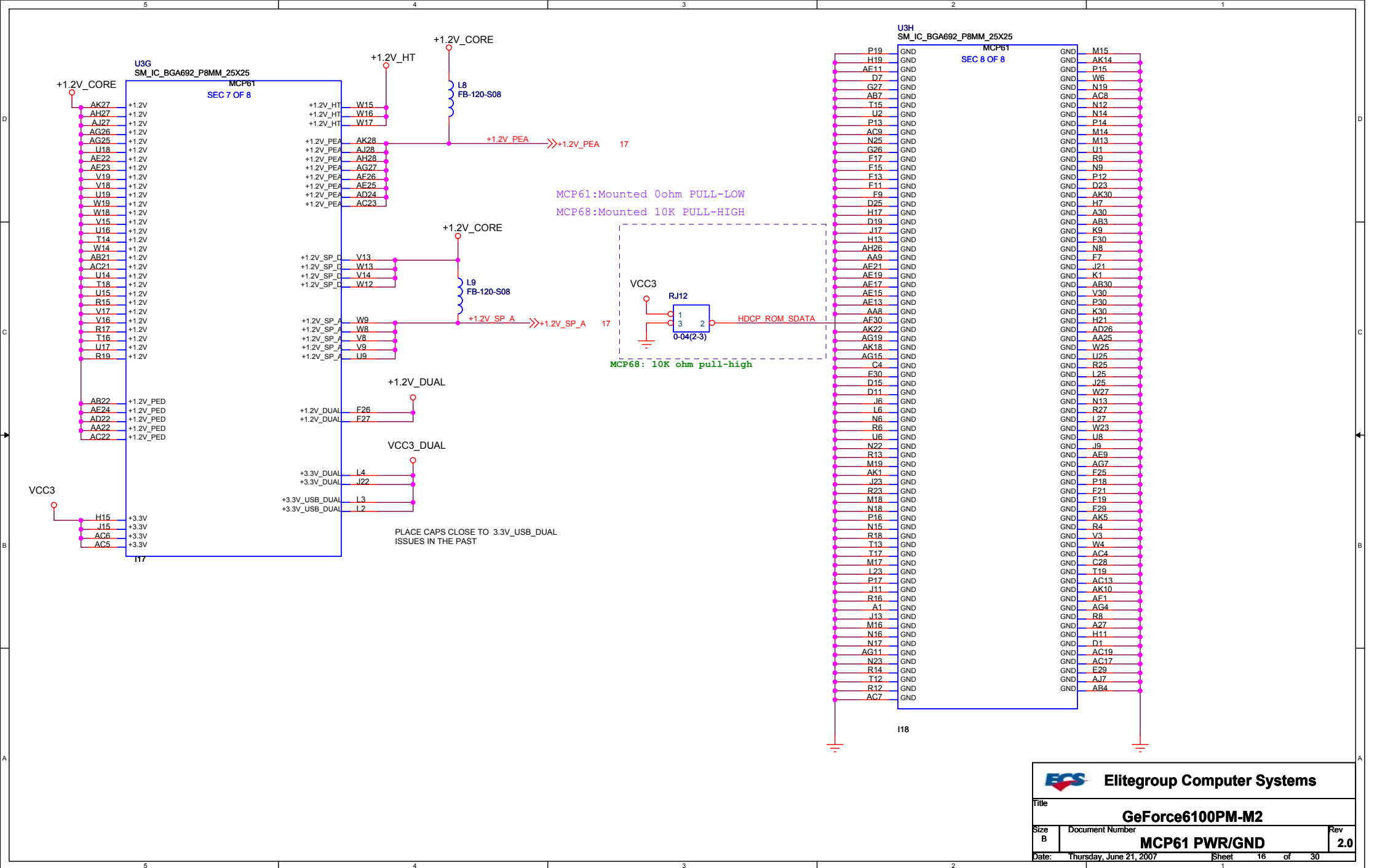


GeForce6100PM-M2			
Size B	Document Number	Rev	
	MCP61 PCI-E X1/RGMII/DAC	2.0	
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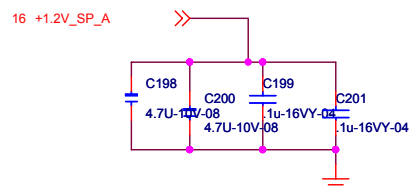
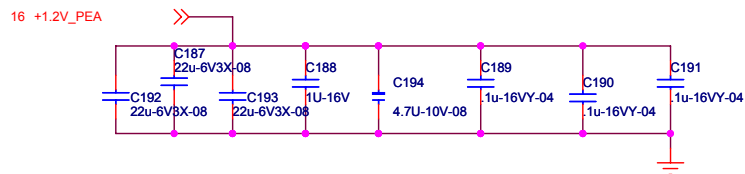
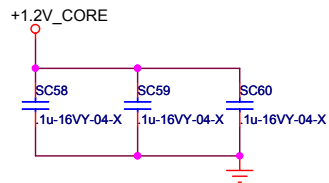
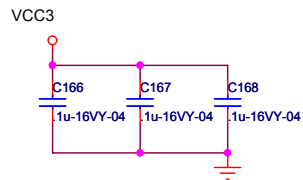
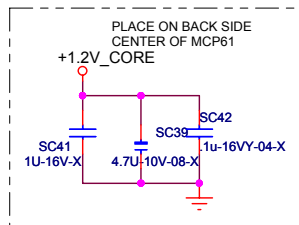


USB0~3 --> BACK CONNECTORS
USB4~11 --> ON-BOARD HEADER

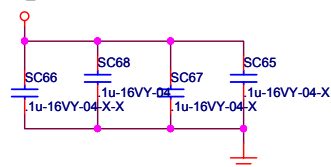




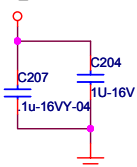
MCP61/8 DECOUPLING/EMI



VCC3_DUAL



+1.2V_DUAL



MCP61 INTERNAL PULL-UP/DWN'S

PE0_PRSTX16* PE0_PRSTX8*	10K PU TO 3.3V 10K PU TO 3.3V
PE1_PRST* PE2_PRST*	10K PU TO 3.3V 10K PU TO 3.3V
PE1_CLKREQ*	10K PU TO 3.3V
PCI_PME*/GPIO_30	8.2K PU TO 3.3V_DUAL
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 LPC_DRQ1/LPC_CS* LPC_DRQ0* LPC_SERIRQ	8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 10K PU TO 3.3V
HDA_SDATA_IN1/GPIO_23/MGPIO_0 HDA_SDATA_IN0/GPIO_22	10K PD TO GND 10K PD TO GND
JTAG_TMS JTAG_TRST* JTAG_TDI	10K PU TO 3.3V 10K PD TO GND 10K PU TO 3.3V
A20GATE PE_WAKE* EXT_SMIF/GPIO32 THERM/GPIO_59 KBRDRSTIN*/GPIO_58 RI*/GPIO_33 SIO_PME*/GPIO_31/MGPIO_2 PWRBTN* RSTBTN*	10K PU TO 3.3V 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V 10K PU TO 3.3V 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL

MCP61 SPI CLK STRAP

SPI_DO | SPI_CLK

00 = 500KHZ
01 = 1.8MHZ
10 = 2.5MHZ
11 = 25MHZ

*DEFAULT

MCP68 SPI CLK STRAP

SPI_DO | SPI_CLK

00 = 31MHZ
01 = 42MHZ
10 = 25MHZ
11 = 1MHZ

*DEFAULT



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Title

GeForce6100PM-M2

Size

Document Number

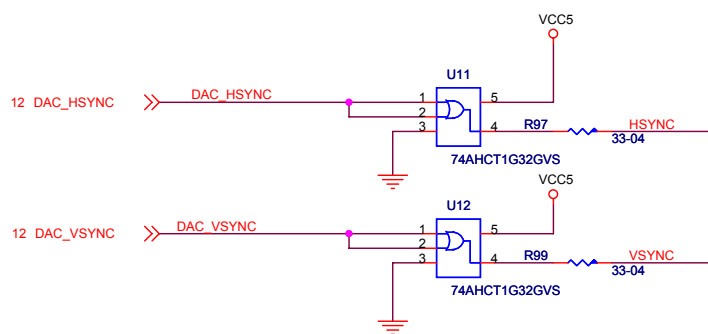
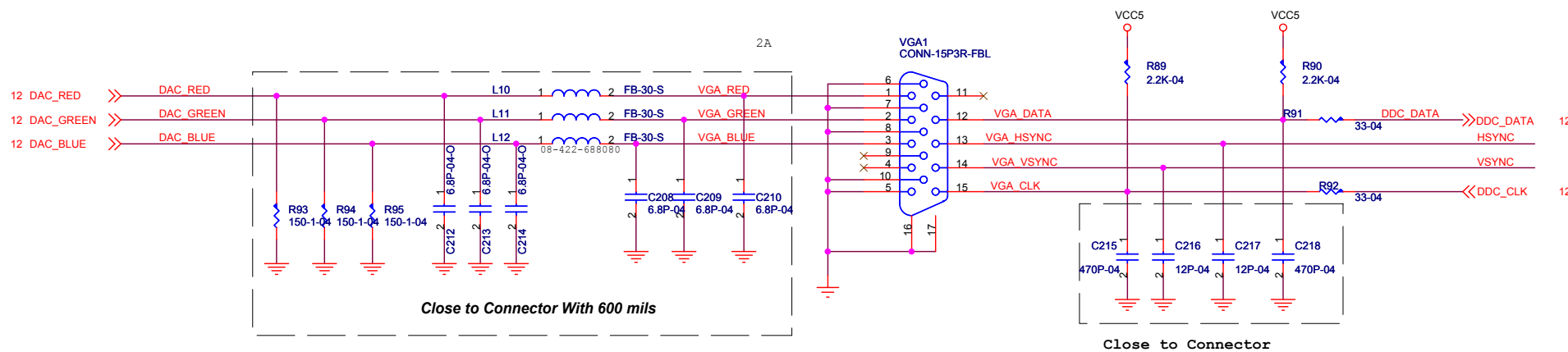
MCP61 SATA / IDE / CONN


Rev

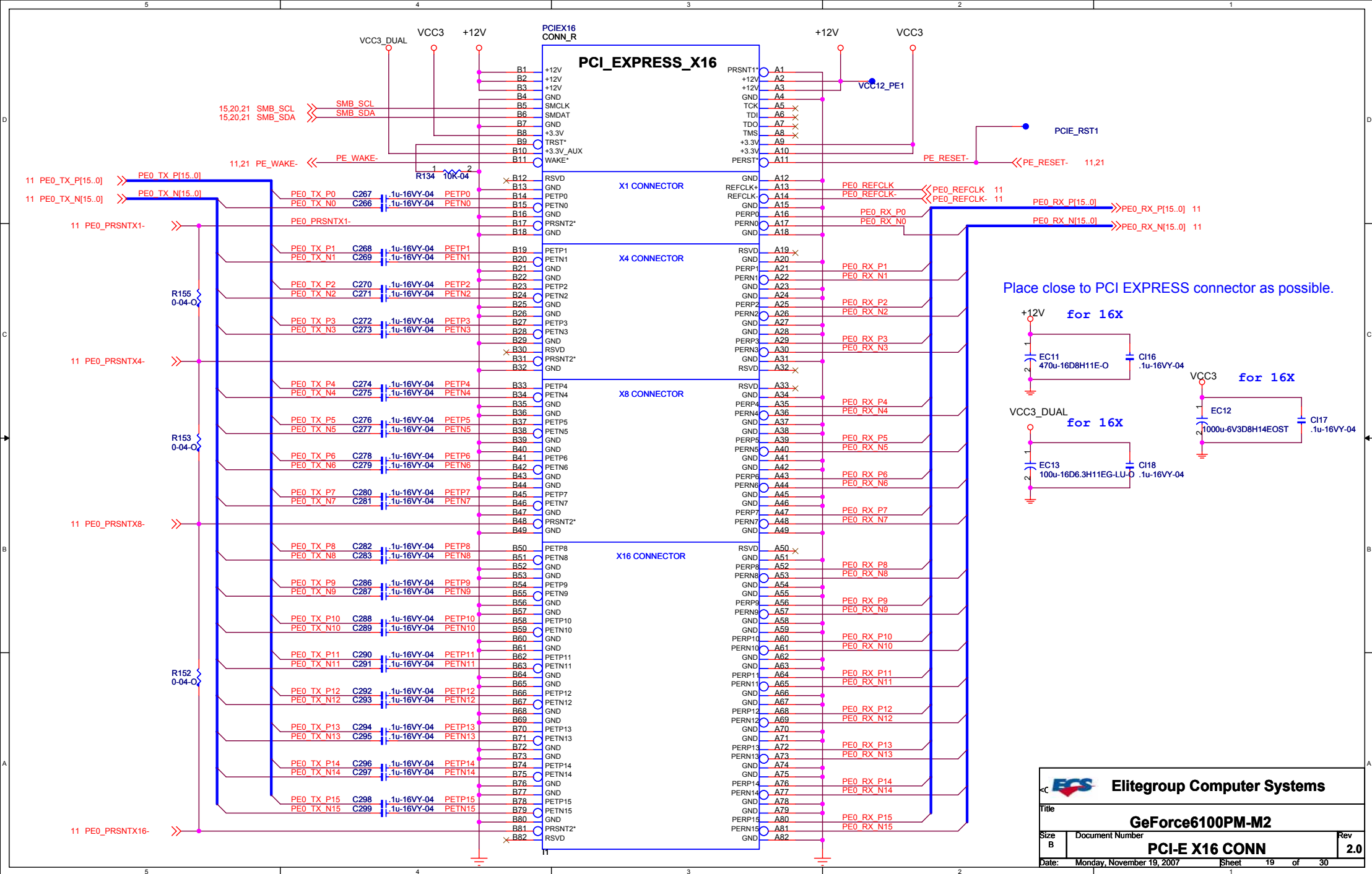
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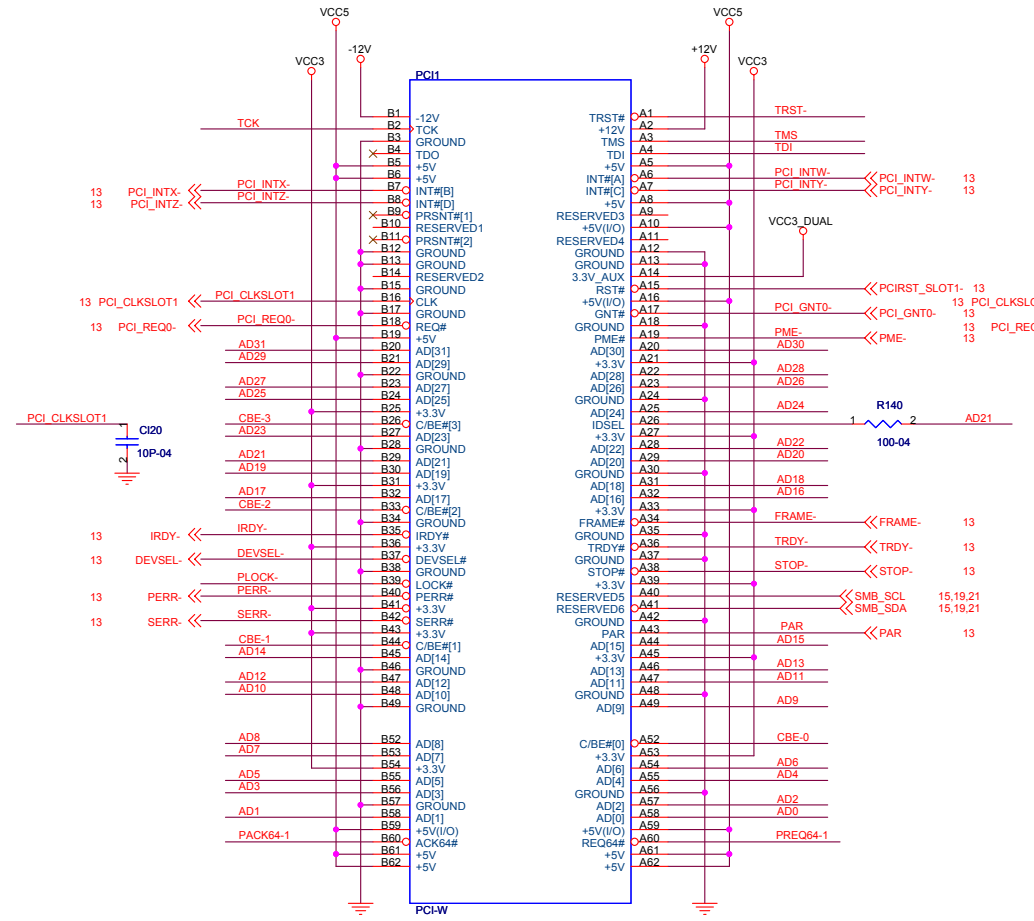
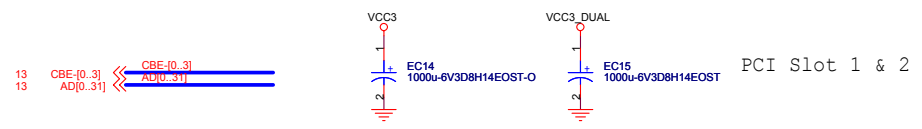
Date: Thursday, June 21, 2007

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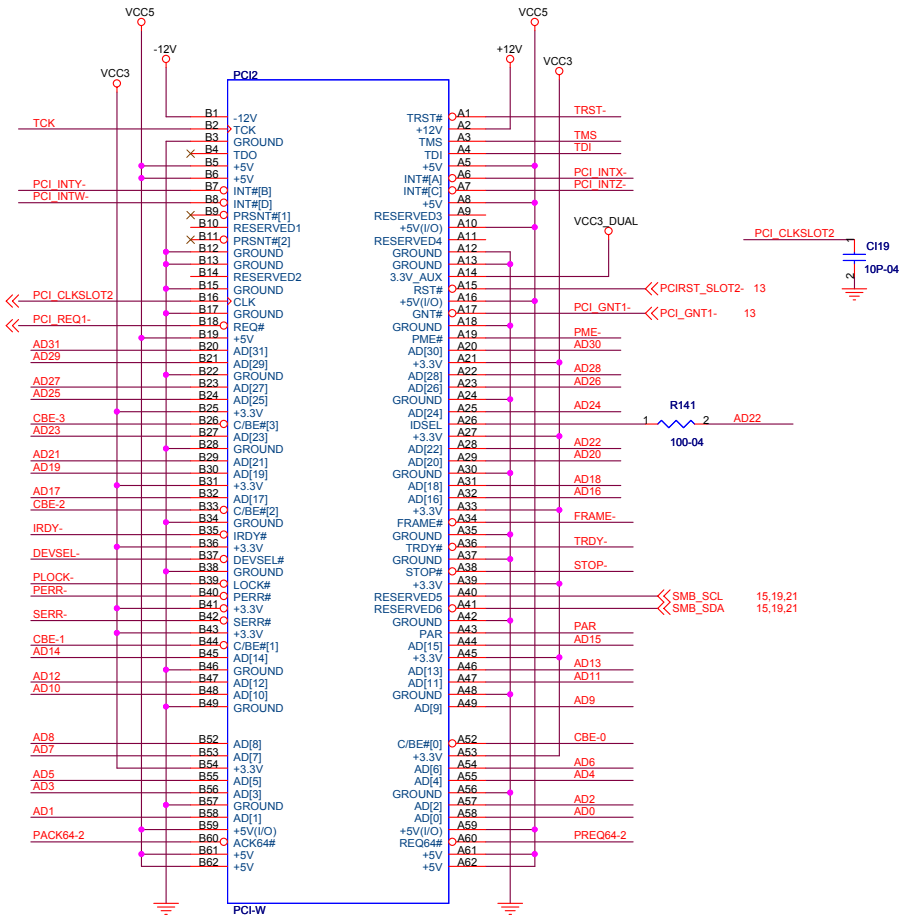


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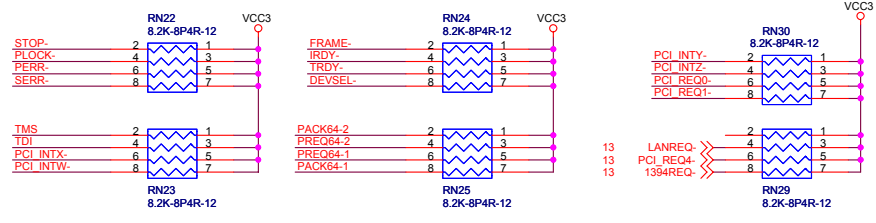




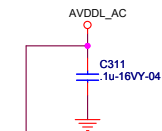
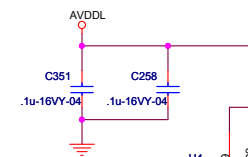
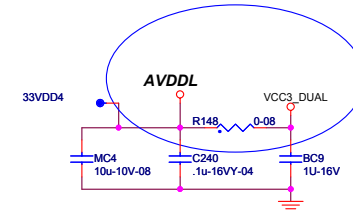
AD21 WXYZ



AD22 XYZW



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A diagram of a 16-pin DIP package. The package is rectangular with 16 pins (8 on each side). A central label indicates a pitch of 150 mil.

The image contains two schematic diagrams for SPI-ROM components. The top diagram is for the SPI-ROM-S-4M-0 (208mil width) in an SMT package. It shows a 4-pin package with pins 1, 2, 3, and 4. Pin 1 is connected to SPI_CS, pin 2 to SPI_DO, pin 3 to WP_ROM, and pin 4 to GND. The package is connected to VCC3_DUAL and R69 (4.7K-04). The bottom diagram is for the SPI-ROM-D-8M in a DIP package. It shows an 8-pin package with pins 1 through 8. Pins 1, 2, 3, and 4 are connected to SPI_CS, SPI_DO, WP_ROM, and GND respectively. Pins 5, 6, 7, and 8 are connected to GND, SCK, SI, and HOLD- respectively. The package is connected to VCC3_DUAL and R69 (4.7K-04).

SMT Package (SPI-ROM-S-4M-0)

Pin	Signal
1	SPI_CS
2	SPI_DO
3	WP_ROM
4	GND

DIP Package (SPI-ROM-D-8M)

Pin	Signal
1	SPI_CS
2	SPI_DO
3	WP_ROM
4	GND
5	GND
6	SCK
7	SI
8	HOLD-

10/100: 10-084-022622

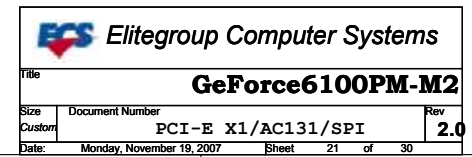
Diagram illustrating a network topology with 10 nodes (1-10) and their connections. The nodes are arranged in a grid-like structure with additional connections to external nodes (11-13).

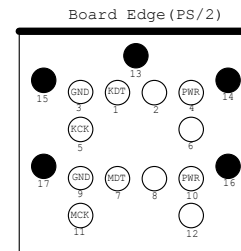
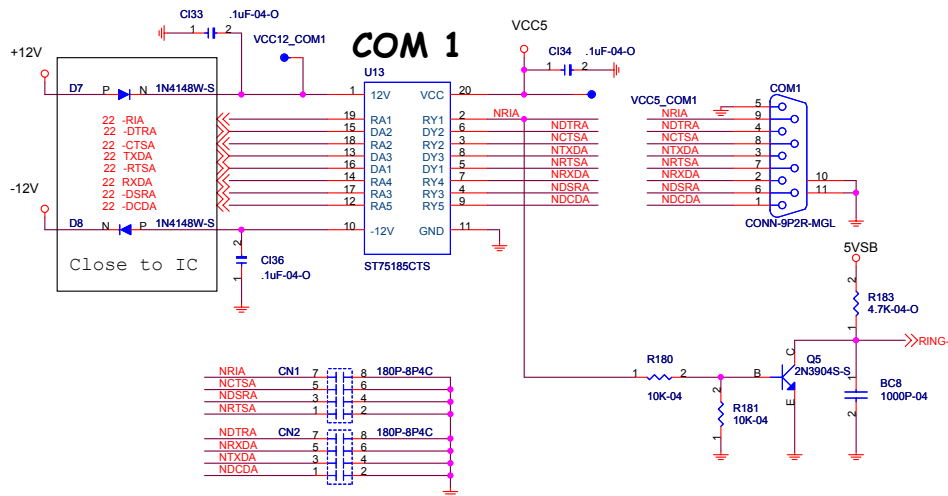
Node connections (Edges):

- Node 1 is connected to Node 2, Node 3, and Node 4.
- Node 2 is connected to Node 1, Node 3, and Node 8.
- Node 3 is connected to Node 1, Node 2, and Node 4.
- Node 4 is connected to Node 1, Node 3, and Node 7.
- Node 5 is connected to Node 6, Node 7, and Node 8.
- Node 6 is connected to Node 5, Node 7, and Node 8.
- Node 7 is connected to Node 5, Node 6, and Node 8.
- Node 8 is connected to Node 5, Node 6, and Node 7.
- Node 9 is connected to Node 10 and Node 11.
- Node 10 is connected to Node 9 and Node 11.
- Node 11 is connected to Node 9 and Node 10.
- Node 12 is connected to Node 13 and Node 14.
- Node 13 is connected to Node 12 and Node 14.
- Node 14 is connected to Node 12 and Node 13.

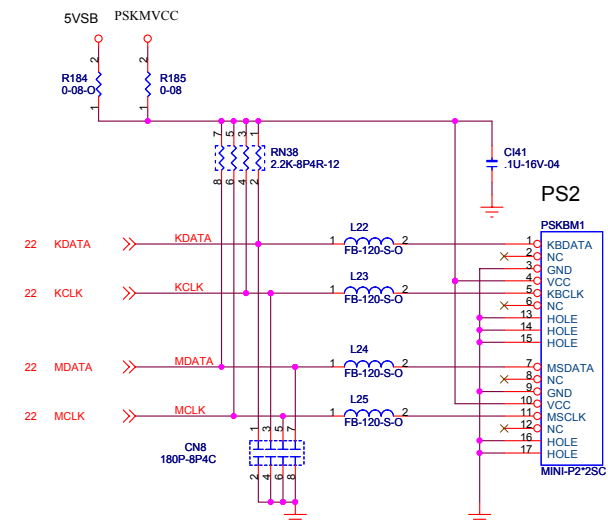
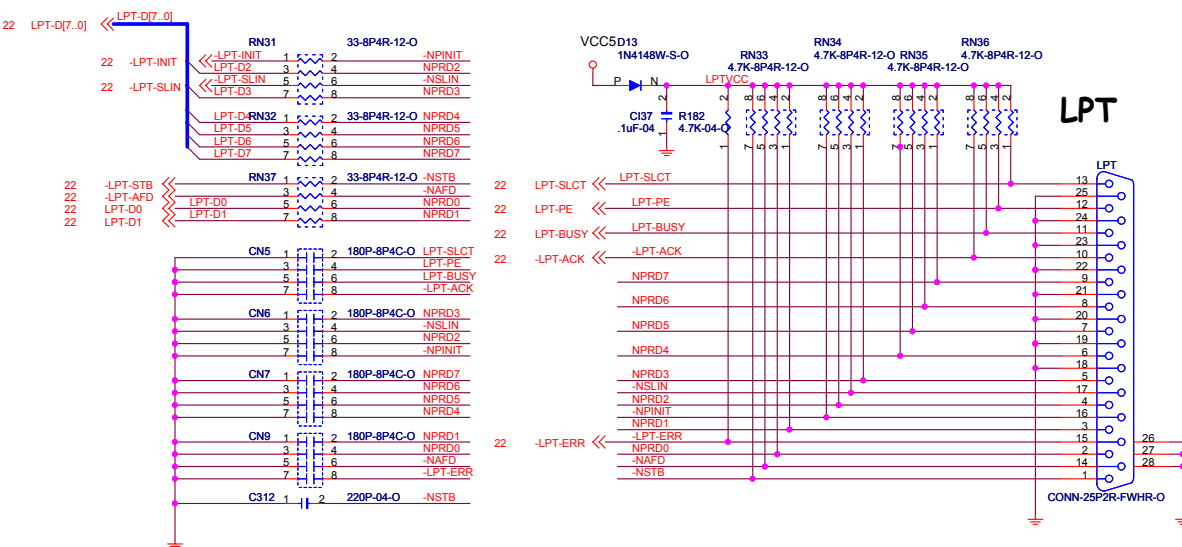
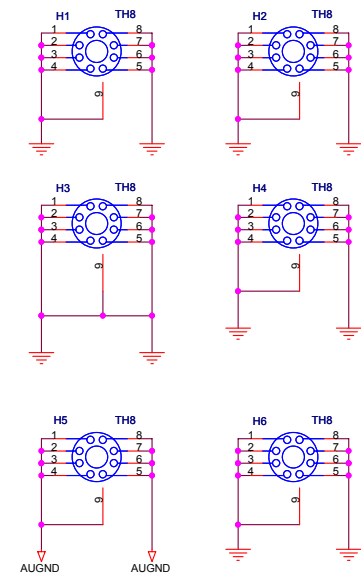
Legend for Node Types/Status:

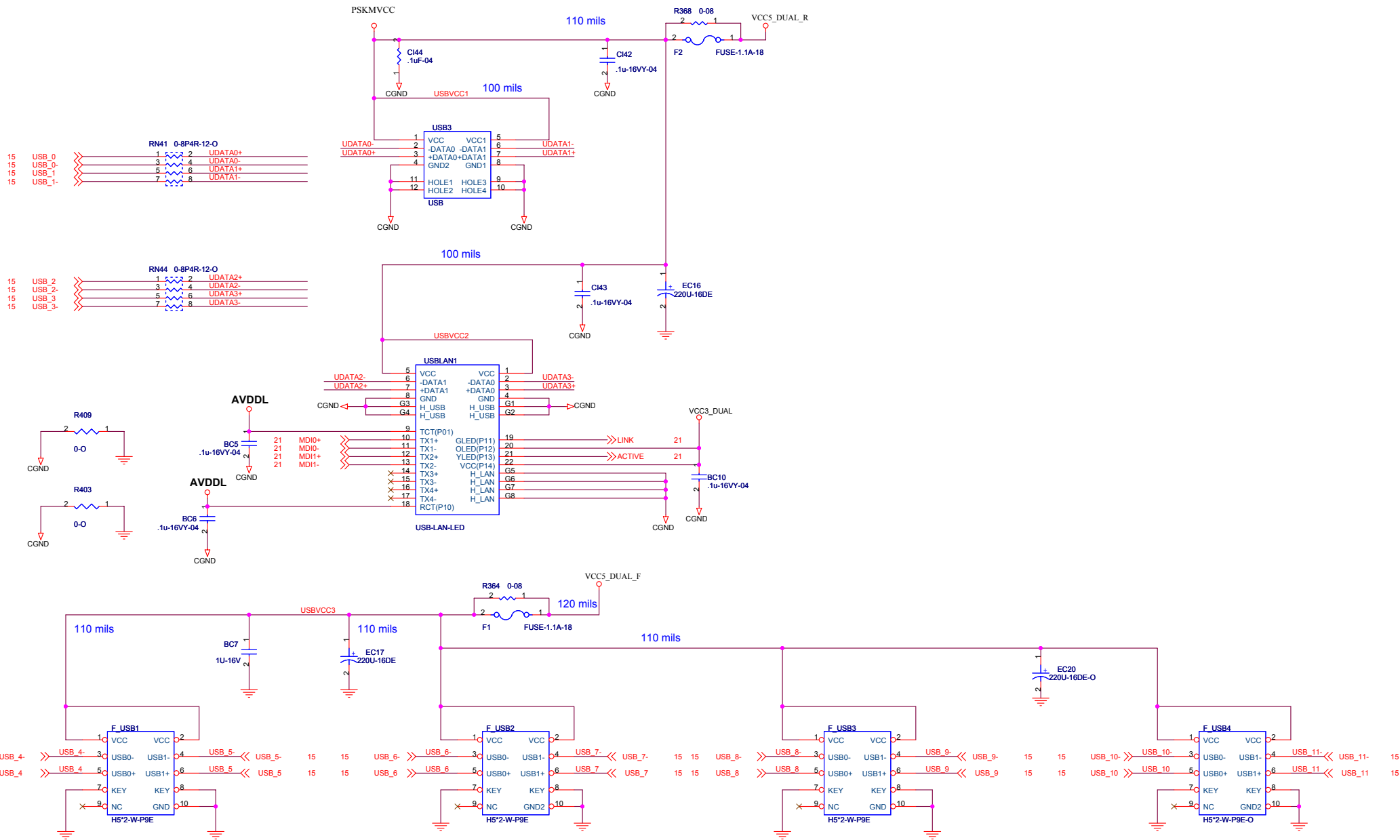
- GREEN: Node 9
- ORANGE: Node 10
- YELLOW: Node 12



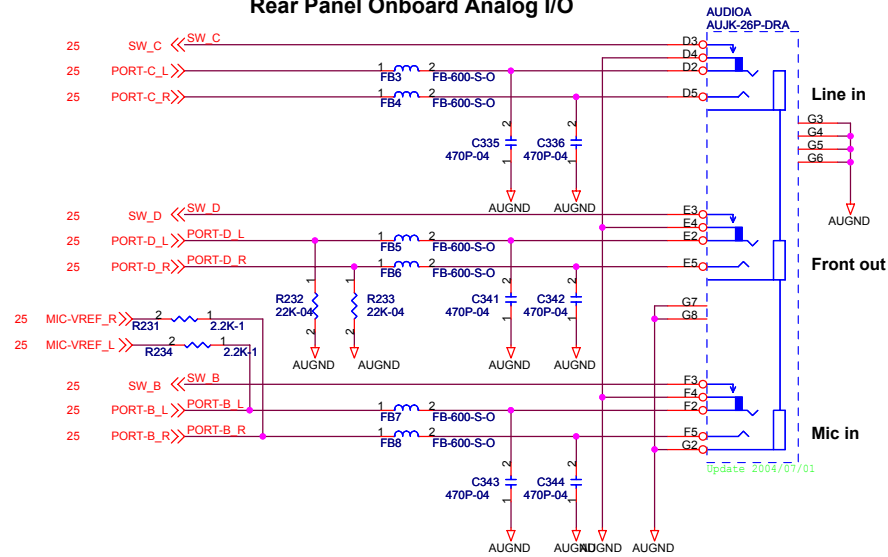


Top View

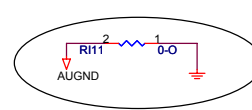
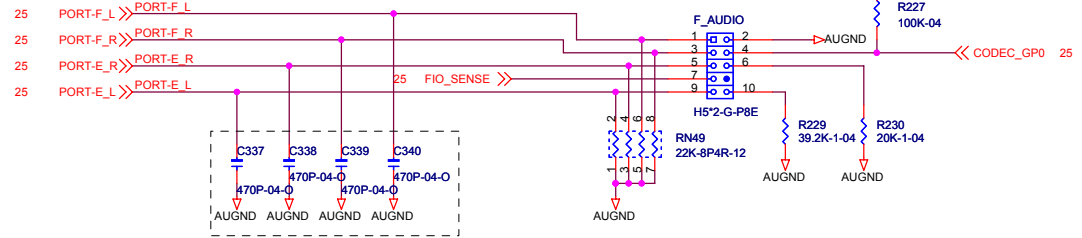
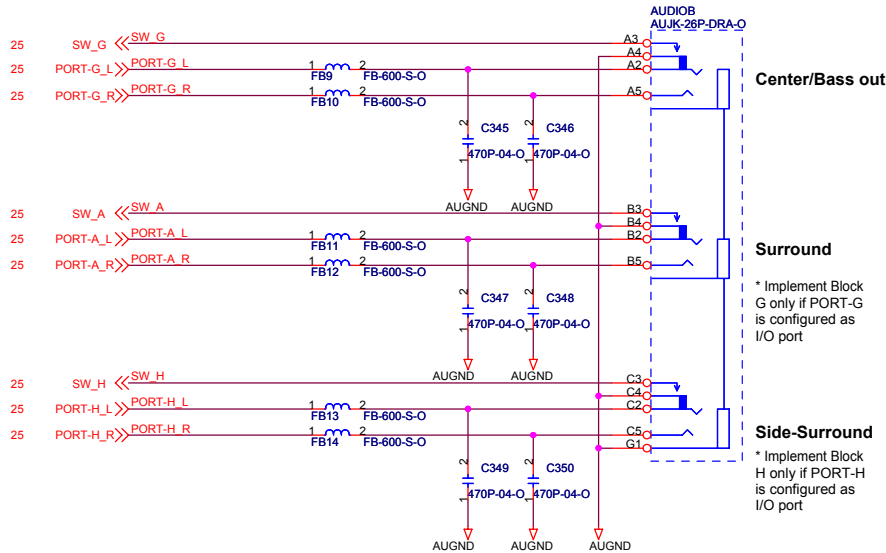




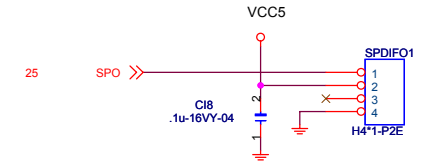
Rear Panel Onboard Analog I/O



Rear Panel (Optional Rear Audio Panel)



SPDIF Out



The schematic should consist with PINs define of I/O connector.

TOP VIEW

